REMARKS

Claims 1, 5, 13, 17, 25, 29-30, 33, 35-36, 38-39, 42, and 44, all the claims pending in the application, stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1, 5, 13, 17, 25, 29-30, 33, 35-36, 38-39, 42, and 44 stand rejected under 35 U.S.C. §102(b) as being anticipated by Ker, et al. ("Automatic Methodology for Placing the Guard Rings into Chip Layout to Prevent Latchup in CMOS IC's," IEEE, Vol. 1, September 2001, pp. 113-116), hereinafter referred to as Ker. Applicants respectfully traverse these rejections based on the following discussion.

Applicants traverse the rejections because the prior art of record fails to teach or suggest the claimed features of displaying logic devices and a guard ring symbolically and schematically in a single integrated display (independent claims 1, 13, and 25). Although the Office Action argues that the "layout of circuit design" of Ker "must be constructed from a schematic", the schematic is not *displayed* along with the layout view "in a single integrated display".

The claimed invention provides a method of displaying at least one guard ring within a hierarchical integrated circuit design having logic devices, a parameterized cell, and the guard ring. In the rejection, the Office Action argues that Ker discloses many features of the claimed invention. However, Ker does not disclose displaying logic devices and the guard ring symbolically and schematically in a single integrated display.

Conversely, as shown in FIG. 14 of Applicants' disclosure, item 141 illustrates logic devices displayed schematically, item 142 illustrates a guard ring displayed symbolically, and item 140 illustrates a combination of item 141 and 142; i.e., the logic devices and guard ring displayed symbolically and schematically in a single integrated display. Instead, Ker merely displays "layout views" showing component "shapes" without schematics. FIGS. 1-3 of Ker do not provide a single integrated display that has *both* schematic *and symbolic* representations of a guard ring and logic devices. Moreover, FIG. 4 of Ker does not provide a single integrated display that has *both* symbolic *and schematic* representations of a guard ring and logic devices. Furthermore, nothing within Ker discloses a hierarchical integrated circuit design having a parameterized cell and a guard ring. Instead, Ker merely discloses an integrated circuit design having multiple guard rings. Therefore, as explained in greater detail below, Applicants respectfully submit that the prior art of record does not teach or suggest the claimed invention.

The Office Action argues that Figures 4(a) and 4(b) of Ker disclose displaying logic devices and a guard ring symbolically and schematically in a single display (Office Action, p. 3, item. 5). Such features are defined in independent claims 1 and 25 using similar language.

Applicants respectfully traverse this rejection and submit that Figures 4(a) and 4(b) of Ker do not disclose displaying logic devices and a guard ring *schematically*. Figures 4(a) and 4(b) of Ker do not illustrate the functional device components schematically; instead, "layout views" showing component "shapes" are displayed *without schematics*.

Specifically, as provided in page 114, column 1, section 2.1 of Ker, to provide the connection from the power lines to the guard rings, a cell called as "instance" was setup in a cell library. The "shapes of such instances in different CMOS processes are shown in Fig. 4(a) and 4(b)". Further, the Figure description on page 114, column 2, describes "Layout of the instances". *However, FIGS. 4(a) and 4(b) do not display the instances symbolically and schematically.* FIGS. 4(a) and 4(b) lack a schematic representation of the guard ring and a schematic representation of the logic devices. The Office Action argues that the instances of FIGS. 4(a) and 4(b) "must be constructed from a schematic" (Office Action, p. 7, para. 1). However, such a schematic is not displayed in FIGS. 4(a) and 4(b) in combination with a symbolic representation of the guard ring and logic devices in a single integrated display. Applicants further note that the circuit illustrated in Fig. 1(b) is not displayed to the user in a display component.

To the contrary, Figure 14 of Applicants' disclosure illustrates a schematic view of logic devices (141) and a symbolic view of a guard ring (142). Additionally, Figure 14 illustrates displaying logic devices and the guard ring symbolically and schematically in a single display (140).

Accordingly, Applicants submit that unlike the claimed invention, Ker does not disclose displaying logic devices and the guard ring symbolically and schematically in a single display. Instead, "layout views" showing component "shapes" are displayed in Ker without schematics. Therefore, it is Applicants' position that Ker fails to disclose the claimed feature of "displaying said logic devices and said guard ring symbolically and

schematically in a single integrated display" as defined in independent claims 1, 13, and 25.

In addition, Applicants traverse the rejections because Ker fails to disclose displaying a guard ring within a hierarchical integrated circuit design, wherein the hierarchical integrated circuit design has a parameterized cell and at least one guard ring. Such features are defined in independent claim 13 using similar language.

More specifically, as discussed in paragraph 0048 of Applicants' disclosure, FIG. 5 is a flowchart that illustrates that the invention first identifies the type of circuit (and the type of ESD protection) 50. This allows the invention to create a parameterized cell (P-cell) 51. The invention then selects the appropriate type of guard ring and places the guard ring within the P-cell 52. *The combined guard ring and P-cell are produced and can be used in a hierarchical circuit design 53.* As further discussed in paragraph 0056 of Applicants' disclosure, FIG. 13 illustrates a hierarchical structure used for the graphical, circuit schematic, or symbol hierarchy. In FIG. 13, *the guard ring P-cell 131 and hierarchical ESD P-cell 132 are combined to form the ESD guard ring hierarchical design 130.*

Moreover, as discussed in paragraph 0051 of Applicants' disclosure, FIG. 7 is a graphical illustration of an input node ESD P-cell that can be used in a hierarchical design. This *parameterized cell* includes voltage lines VDD 70 and VSS 72 P+/N- well diodes 71 that are positioned between the stretch lines 73. This parameterized cell can be auto-generated and actually contains two primitive parameterized (twin diodes). FIG. 8 illustrates the same structure as that shown in FIG. 7 and includes the *guard ring 80*. In

this implementation, the new parameterized cell is modified in that it is now contain all the data information of the parameterized cell guard as well as the ESD parameterized cell.

To the contrary, nothing within Ker discloses a hierarchical integrated circuit design having a parameterized cell and a guard ring. Instead, Ker merely discloses an integrated circuit design having guard rings. Although the Office Action argues that Ker teaches the use of double guard rings (Office Action, p. 4, item 6), nothing within Ker discloses a hierarchical integrated circuit design including such guard rings and a parameterized cell.

In support of its arguments, the Office Action references FIGS. 4(a) and 4(b) of Ker, wherein the Office Action asserts that Ker discloses multiple guard rings. However, the "layout of the instances" shown in FIGS. 4(a) and 4(b) of Ker does not include a hierarchical integrated circuit design. Moreover, the "layout of the instances" shown in FIGS. 4(a) and 4(b) of Ker does not include a parameterized cell.

Therefore, it is Applicants' position that Ker fails to teach or suggest the claimed feature of "displaying at least one guard ring within a hierarchical integrated circuit design having logic devices, a parameterized cell, and said at least one guard ring" as defined by independent claim 13.

Applicants traverse the rejections because the prior art of record fails to teach or suggest the claimed feature of displaying logic devices and a guard ring symbolically and schematically in a single integrated display (independent claims 1, 13, and 25). The Office Action argues that such features are disclosed in Ker because the "layout of circuit

design" shown in Fig. 4 of Ker "must be constructed from a schematic" (Office Action, p. 7, para. 1).

Applicants submit that whether or not a schematic is utilized to construct the layout view shown in Fig. 4 of Ker is irrelevant because the schematic is not *displayed* along with the layout view "in a single integrated display".

The claimed invention defines the positive step of "*displaying* said logic devices and said guard ring symbolically and schematically in a *single integrated* display" (independent claims 1, 13, and 25 (emphasis added)). To the contrary, nothing within Ker discloses displaying the "layout" and the schematic referenced by the Examiner in a single integrated display.

In addition, the Office Action argues that schematics are shown in Figs. 1-3 of Ker (Office Action, p. 7, para. 1). The fact that multiple figures are referenced supports Applicants' position that logic devices and the guard ring are not displayed in a *single integrated* display. Specifically, the Office Action must reference three *different* figures to illustrate schematic displays and symbolic displays. The Office Action is unable to point to a *single* figure that has *both* schematic *and* symbolic representations of the guard ring and logic devices displayed in a *single integrated* display. To the contrary, as illustrated in FIG. 14 of Applicants' disclosure, item 140 displays logic devices and a guard ring *both* symbolically *and* schematically in a *single integrated* display.

Therefore, it is Applicants' position that Ker does not teach or suggest many features defined by independent claims 1, 13, and 25 and that such claims are patentable over the prior art of record. Further, it is Applicants' position that dependent claims 5,

17, 29-30, 33, 35-36, 38-39, 42, and 44 are similarly patentable, not only because of their dependency from a patentable independent claims, but also because of the additional features of the invention they defined. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1, 5, 13, 17, 25, 29-30, 33, 35-36, 38-39, 42, and 44, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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